Efficient Design of Bit Parallel Multiplication based Radix-4 Multipath Delay Commutator (R4mdc) FFT

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Abstract

This paper presents the Fast Fourier Transform (FFT) techniques for converting a signal in the time domain to the frequency domain. The advent of Fast Fourier Transform (FFT) method has greatly extended our ability to implement the Fourier methods on digital computers. FFT is an algorithm that speeds up the calculation of Discrete Fourier Transform (DFT). Pipelined FFT have features like simplicity, modularity and high throughput. Radix-2 Multi-Path Delay Commutator (R2MDC) FFT is the best frequency transformation architecture for FFT calculation. However it requires more delay elements to provide desired frequency transformation functions. To overcome this problem, Radix-4 Multi-Path Delay Commutator (R4MDC) has been designed in this paper. In addition, structure of Bit Parallel Multiplication (BPM) has been modified to alleviate the performance of twiddle factor multiplier of FFT architecture. Modified BPM structure has utilized only little hardware to perform the twiddle factor multiplication. Finally, Modified BPM structures have been incorporated into R4MDC FFT structure for alleviating the performances of frequency transformation process. Design of proposed methods has been validated by using ModelSim 6.3C and Synthesis results has been evaluated by using Xilinx 12.4i (Family: Spartan 3, Device: Xc3s200, Package: PQ208, Speed: -5) design tool.

Keywords: Fast Fourier Transform (FFT), Radix-2 Multi-Path Delay Commutator (R2MDC), Bit Parallel Multiplication (BPM), Radix-4 Multi-Path Delay Commutator (R4MDC), Very Large Scale Integration.
References


